CQ.P. Code: 19EC4205 **R19**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

M.Tech I Year I Semester Regular Examinations Jan 2020

VERILOG HDL

(VLSI)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Explain hardware modeling and Verilog primitives.	**6M**
	b	Write a Verilog program for 16x1 MUX using Structured Implicit model.	**6M**
		OR	
2	**a**	Explain the terms "Hardware Encapsulation" and "Hardware modeling" with suitable example using Verilog HDL.	**6M**
	b	Write Verilog HDL structural model for a full sub tractor using NAND gates.	**6M**
		UNIT-II	
3	**a**	Write a brief short note on User Defined Primitives in Verilog.	**6M**
	b	Explain Built-In Constructs for Delay in Verilog.	**6M**
		OR	
4	**a**	Compare the combinational behavior and sequential behavior of user defined primitives.	**6M**
	b	Explain the Verilog model for net delay and module paths and delays.	**6M**
		UNIT-III	
5	**a**	How intra assignments delay control, event-based timing control takes place in Verilog HDL?	**6M**
	b	Write program for Moore machine using behavioral models.	**6M**
		OR	
6	**a**	Explain the behavioral descriptions for simulation of simultaneous procedural assignment used in Verilog HDL with suitable example.	**6M**
	b	Explain the Indeterminate Assignments and Ambiguity in Verilog.	**6M**
		UNIT-IV	
7	**a**	Draw the block diagram for HDL based synthesis explain each block in detail.	**6M**
	b	Discuss about RTL synthesis.	**6M**
		OR	
8	**a**	Explain the synthesis of user defined function.	**6M**
	b	Write a program for synthesis of case and conditional.	**6M**
		UNIT-V	
9	**a**	Discuss the importance of MOS Transistors in Switch level models.	**6M**
	b	Write and verify a switch level model of a Three-input static CMOS NOR gate.	**6M**
		OR	
10	**a**	Draw & explain the circuit diagram of CMOS switch with a program.	**6M**
	b	Write a program for NMOS Three-input NOR gate.	**6M**

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